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New Test Sequencing Instruments Lower Cost of Test for Device Manufacturers

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Business Pressures Challenge Test Engineers

Most electronic manufacturers face a common set of business problems. Global competition exerts downward pressure on prices, while increasing the features and functionality of products. This takes place within ever-shortening product life cycles. Narrowing profit margins then drive efforts to reduce product costs wherever possible. This includes the cost of testing, which tends to grow with product complexity.

These forces are a significant challenge to test and production engineers. The integration of analog, digital, and even RF circuitry on a single System-On-a-Chip (SOC) means more circuitry in less space and higher pin counts on each new generation of devices. There is a similar push in discrete devices, with the consolidation of multiple components on a single chip for higher density and smaller size. Higher pin counts require more test channels to maintain acceptable throughput, while test system density must also increase within limited production space. These factors push the limits of test technology.

In addition, the concentration of testing at the functional level in final production, as we often see today, can hurt profits because failed units carry a heavy burden of sunk production costs. This calls for a shift to more up-front testing to eliminate bad parts earlier in the process. Unfortunately, “big iron”

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end-of-line functional test systems generally are not efficient solutions for testing components and modules in the early stages of production.

Currently, production ATE systems can be categorized as bulky, high cost mainframe-based systems, slow instrument-based systems using PC control, or fast instrument-based systems that are extremely complex to develop. None of these solutions are optimized for either front-end or back-end processes. In order to remain price competitive, manufacturers need test techniques, instruments, and systems that allow them to minimize their cost of testing and the ongoing cost of equipment ownership. In many cases, they are looking for ways to minimize ownership costs by improving the performance of existing test stands, with the aim of having them take on more of the test burden. This will help reduce the amount of high cost, end-of-the-line testing. In short, test system designs must:

- Increase throughput (shorten test time).
- Minimize test stand footprints and rack space.
- Reduce development time.
- Offer lower cost of ownership.

Matching Test Equipment Architecture to the Application

In facing these challenges, production test engineers have to survey the ATE landscape thoroughly to find new hardware and software structures that provide the best value for their required test functions (i.e., seek the most bang for the buck). The most cost-effective equipment depends, of course, on the application specifics. However, within most production environments, a common need is for a set of repetitive component (or module) test sequences that apply a voltage or current, measure the DUT response, compare it to acceptable limits, and make a pass/fail decision. This is particularly true in the early stages of production. Naturally, accurate low noise source and measure capabilities are mandatory for these applications.

Simple two- to four-pin devices. This DUT category includes such things as circuit protection devices, diodes, LEDs, transistors, linear regulators, DC-DC converters, opto isolators, MEMs switches, and relays. For two-terminal devices, a fairly simple source-measure protocol can be used. Three- and four-terminal devices require more complex testing, and fast transient response on two test channels to generate accurate I-V curves. With the latest component handlers incrementing as fast as 10ms per part, instrument speed can be a test system bottleneck.

Component arrays. Examples include resistive chip arrays, Transient Voltage Suppression (TVS) arrays, integrated ferrite beads, and flip-chip arrays. The tests performed on these devices are the same as those performed on the discrete versions of these components. However, all individual devices must test good before an array can pass. For high throughput, array production requires parallel, multi-channel testing.

IC/RFIC/component-on-wafer testing. This category encompasses a wide variety of complex devices. In the early stages of production, they typically require measurements of quiescent current and leakage at nanoamp levels. This level of sensitivity is driven by low power designs that help extend battery life. In addition, this testing usually includes a simple set of DC measurements to check the basic functionality of all devices on a wafer. There are thousands of devices per wafer, so fast multi-channel testing is a must.

Other complex devices/modules. Some examples include power supplies, data acquisition cards, RFIC power amplifiers, and hybrid ICs. Such testing requires diverse instruments and measurements that can range from DC to RF. It often requires tight timing between source-measure sequences and multiple instruments to characterize the DUTs accurately. Scalable instruments and test equipment modules are usually needed in the construction of a customized system with a relatively large number of parallel channels.

Typical Test Equipment Architectures

When contemplating production test equipment, it is helpful to think in terms of the three broad categories alluded to earlier:

- Single box/single channel I-V solutions
- Parallel I-V test systems
- Scalable multi-channel systems

Single box/single channel I-V solutions often are acceptable in less cost-sensitive applications where the lower speed of a sequential source-measure protocol can be used. Multiple source-measure units (SMUs) may be used with or without switch matrixes to form multi-channel systems, but this arrangement has limited rack density and system throughput. In smaller systems, SMUs are typically used under PC control via GPIB and/or external trigger lines. However, some of them have an internal program memory that allows a test sequence to be stored and executed without PC control, which cuts down on relatively slow GPIB traffic. Frequently, users develop test execution applications for the PC controller

that encompass SCPI command calls, which are pretty much a necessity when an SMU has limited or no program memory capability.

Parallel I-V systems are designed for multiple DUT testing or for multi-channel testing of more complex devices. Depending on the DUT, speed could be limited by the instrument, by the application program, or by the time it takes the DUT to settle to a stable response after the source is applied (premature measurements produce inaccurate results). Some of the limitations encountered in the current parallel test system designs include sequential channels as opposed to simultaneous source-measure capability, limited voltage or current range, lack of flexibility, bulky equipment, and high cost (because of overkill in instrument sensitivity or highly customized, made-from-scratch designs).

Scalable systems, unlike the other two architectures, often include diverse instruments to test complex devices. The two most common types of scalable multi-channel system are (a) integrated functional testers and (b) I-V test systems built from open API (application program interface) instrumentation. Open API means that instrumentation products are building blocks used to create a customized test solution, as opposed to a parametric tester that is a complete prepackaged system. SMUs are often a core component in both architectures, which may also encompass other equipment like signal generators, oscilloscopes, spectrum analyzers, switching, etc.

While SMUs may be internal modules in parametric and other packaged turnkey testers, broadband instrumentation tends to added as external units. In either case, it's highly desirable that the instruments integrate seamlessly to achieve high speed, multi-channel I-V testing. The advantage of turnkey testers is that much of the hardware and software integration has been done for the user, while still providing a certain degree of flexibility. The downside is relatively high cost. By contrast, open API systems allow a high degree of flexibility, with the potential for much lower cost, depending on the specifics of the application and instrumentation characteristics.

Important Parameters in Lowering Test Costs

At the outset, four system parameters were identified as the key to lower testing costs: shorter test times, reduced development time, smaller footprint or rack space, and lower cost of ownership. Each has a number of facets that should be explored.

Shorter Test Times. After DUTs are loaded into a test fixture or the fixture cycles from one DUT to next, there are several distinct time intervals that make up the greatest portion of total test system cycle time. Depending on system design, these typically include:

- Sourcing time (includes signal transient time).
- DUT settle time.
- Measurement time.
- Range change times (if applicable) for the source-measure instrumentation.
- Trigger delay between separate instruments or between a PC controller and the instruments.
- Data communication times for test commands, digital I/O, triggers (if applicable), and moving collected data to storage or PC memory.
- Program execution time needed to compare measurements with acceptable limits and make a pass/fail or binning decision.
- The test fixture's physical movement and/or electrical switching interval.

Complex DUTs may require the application of multiple source signals and associated response measurements before a test fixture cycles to the next part. The first level of improvement in test time is gained by switching from individual source and measure instruments to an integrated SMU. This cuts down on trigger delay and data communication time between separate instruments and a PC controller. If the SMU has internal program memory, this further reduces data communication time and test program (PC) latencies, because the SMU can run the test sequence from its own memory.

Some SMUs have program memory capable of running up to 100 predefined tests, making limit comparisons, performing conditional test program branching, and working with or without a PC controller during test execution. With that type of design, gaining significant test time improvement is straightforward in a single-channel system. However, it's much more complicated in a multiple SMU system due to the difficulty in managing multiple triggers and the test sequencer. (See sidebar.)

Because of this difficulty, a multiple SMU system design may have a test sequencer that simply uses command cues, i.e., it stores multiple GPIB commands that can be executed with a single SCPI call from the PC controller. This does not provide the logic needed to perform limit testing or make pass/fail decisions on the fly, in which case, there is no DUT handler interface. Therefore, this type of design still involves a great deal of GPIB traffic on the data communications bus. Further more, multiple SMUs may not be used as effectively as

Taking Advantage of SMU Test Sequencing

When switching from individual source and measure instruments to SMUs, the most dramatic gain in throughput is realized by changing the system programming approach. Instead of using PC-based control, the SMU's test sequencer and program memory control the testing. This takes advantage of SMU features that simplify and speed up test execution, which include:

- Four-quadrant operation (acting as either a source or sink, with positive or negative voltage or current.
- Built-in voltage and current sweeping capability.
- Wide dynamic voltage and current ranges.
- Fast transient response (small droop).
- Picoamp sensitivity.
- Resolution as fine as 6½ digits.
- Deep memory (typically up to 100 test sequences).
- Built-in comparator for fast pass/fail testing.
- Digital I/O and connection to component handlers for parts binning.

With all this in a single unit, there is less for a test system designer to integrate. Such features make the SMU's test sequencer extremely powerful, allowing the system designer to do more things with one instrument.

As an example of how an SMU's program memory and test sequencer speed up testing, Keithley Instruments conducted a study in which a single-channel SMU was programmed to execute a typical source-measure sequence internally. This was compared to the same sequence conducted under a PC program running across the GPIB bus.

The test sequence consisted of three simple tests on a diode: V_f, V_{br} and I_r. First, a PC program was written in Visual Basic to control the SMU via GPIB, perform the three tests, and make pass/fail decisions in the VB program. All SMU readings were returned to the PC over the GPIB bus. The resulting system could complete the diode tests and make pass/fail decisions in approximately 250ms.

Next, the system was redesigned to use the built-in test sequencing capability of the SMU. In this case, the PC program pre-configured the instrument once, then the source-measure tests, pass/fail decisions, and component handler control all took place inside the SMU, independent of the PC program and GPIB bus. This redesigned system could complete the testing in about 25ms, i.e., ten times faster than with the other test configuration. The component handler was running at about 180ms per part, so using the SMU test sequencer resulted in a 52% throughput gain. In a production application, this effectively cuts the cost of test in half.

In a single-channel system like the one just described, using the test sequencer is straightforward and works well. In systems that require two or more channels, configuring the test sequencer as well as managing multiple trigger models and external triggering becomes extremely complex, if not impossible. However, a new class of SMU with a test script processor and high speed control bus solves this problem, allowing easy multi-channel scalability and simple programming. These features provide the capability to run a complex, high speed test sequence by sharing all the system's SMU resources. (See the description of Keithley Models 2601 and 2602 elsewhere in the text.)

they could be, i.e., in parallel channel testing. Instead, they are often accessed sequentially, so throughput improvement is marginal.

Today, the fastest SMUs employ a test script processor and high speed control bus that allows master-slave operation of multiple SMUs in a true parallel channel arrangement. This type of design is used in the Keithley Model 2601 and 2602 System SourceMeter® instruments.

Faster Scripting. The use of scripting and script processors are not new; they have long been used to accelerate Web connections and manage various batch processes. Still, their use in the automation of test and measurement instruments has been limited in the past, probably by the way ATE instrumentation evolved. However, in Keithley's new SMU designs, a Test Script Processor (TSP™) is combined with a high speed test sequencer and control bus (TSP-Link™) to allow a multiple SMU system to achieve throughput gains much greater than single-channel sequencers. In the Keithley system, multiple SMUs connected with TSP-Link can be used like they are part of the same physical unit for simultaneous multi-channel testing, as opposed to sequentially accessing multiple SMU channels.

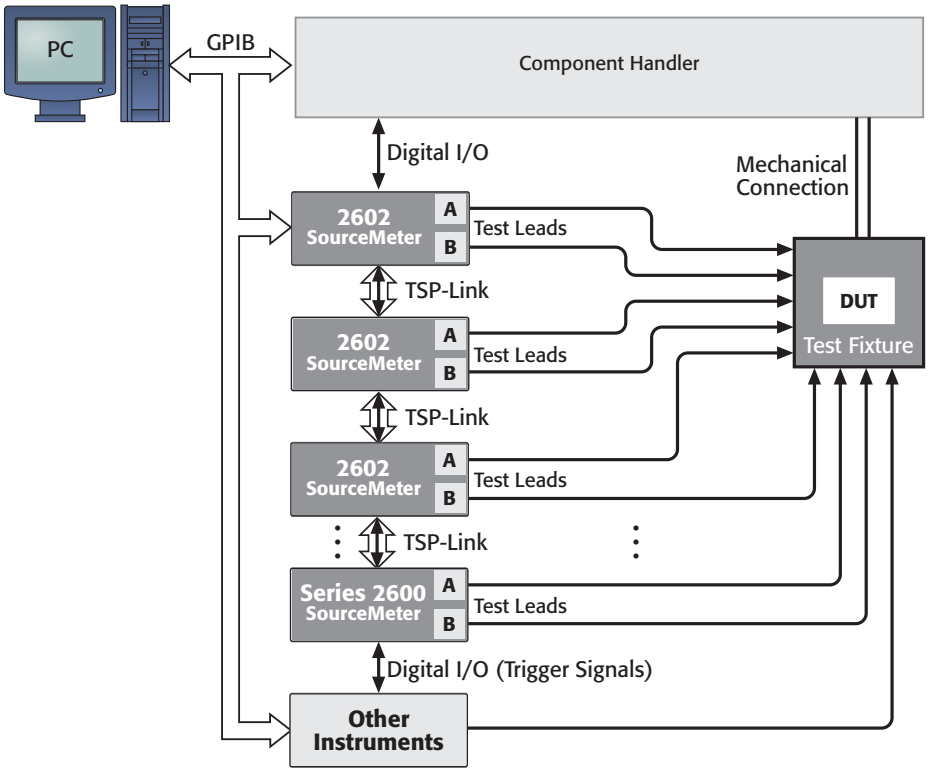

Figure 1. Keithley TSP-based multiple SMU test system.

TSP-Link is, effectively, an external backplane acting as a master-slave trigger synch/inter-unit communication bus, while TSP runs scripts that sequence all aspects of a test. (See ***Figure 1***.) There is no reliance on a PC controller. This design supplies all the capabilities of command cues and source memory, along with the greater automation capability of parallel SMU channels. Any single-unit or multi-unit SMU system can be programmed with TSP to run a single high speed test sequence or any embedded test script. Coordination of multiple SMUs during test sequencing is no longer a challenge. The result is a huge speed improvement over a typical Microsoft® Windows® PC-controlled GPIB instrument system, and comparable to mainframe-based systems.

Reduced Rack Space. The new Keithley units come in a 2U half-rack design that substantially improves rack density. As a practical matter, most systems based on this design will have 16 or fewer channels, but a 128-channel design is possible. This is important as device complexity and pin counts increase the number of test channels required. In this environment, more equipment in less space is critical to lowering production costs. Moreover, a scalable and easily integrated rack-and-stack test system design is now possible.

Shorter Development Time. Test engineer time is a valuable resource, typically costing up to $100,000 per year. In complex test systems, software development has always been a major portion of the total system cost. This is particularly true in proprietary mainframe-based systems. The TSP-based software structure provides a much simpler programming interface for test sequencing in open-API instruments. It allows easy creation of a test sequence across multiple SMUs and channels as if they were all part of a single entity.

For some specialized applications, such as those in semiconductor wafer testing, there are certain advantages to having the pre-written test routines that come with a parametric tester. On the other hand, a TSP-based SMU system is highly flexible and cost-effective. Multiple SMUs can be seamlessly integrated into a scalable "mainframeless" system with the high throughput of a multi-channel, card-based system. Furthermore, evolving test requirements are easily accommodated with a minimum of SMU hardware changes. Users can standardize on one or two SMU models and re-purpose them by simply changing test scripts.

Lower Cost of Ownership. A rack-and-stack SMU system eliminates mainframe overhead and thereby reduces the cost of test system hardware. Re-using SMU hardware as test requirements change also lowers the cost of ownership. A reduction in application software development time has the same effect.

In addition, a smaller test system footprint on the production floor generally equates to lower ownership cost. For example, semiconductor fabricators typically assign a cost per square foot of production space that ranges from $100 to $400. With the rapidly expanding pin counts of today's complex devices, this has significant implications. Higher pin counts often mean that redesigned legacy systems will need two or more racks. Thus, a higher density design can represent a large savings in expensive fabrication space when it allows the test system to remain in one rack. This is especially important in a multi-line production facility that is already full. (No one wants to invest in bricks and mortar to accommodate expanding test requirements.)

Accomplishing the same thing with a card-based mainframe system may not be possible. Typically, mainframes are not cost-effective unless most or all of their card slots are filled.

Other Important SMU Features

In addition to typical SMU features, the Keithley Model 2601 and 2602 System SourceMeter instruments provide new functionality that greatly expands I-V test capabilities. For example, the wide dynamic range associated with SMUs is complemented with seamless range

change capabilities in these new units. Ranging can consume a lot of source-measure time, so seamless range changes significantly speed up test sequences that cover multiple ranges on an SMU.

In addition to a power supply, DMM, and bias source found in most SMUs, these new units have a pulse generator and low frequency arbitrary waveform generator capability that can be applied to each SourceMeter channel. This simplifies complex testing requirements by providing a universal analog I/O pin for a wide range of applications involving active and passive components.

The TSP-Link technology in each SMU employs embedded trigger lines and a 100Mbit serial bus that allows parallel I-V sweeps across multiple units with low trigger jitter, which is critical for high bandwidth applications.

The Keithley TSP uses an uncomplicated command language similar to BASIC. This is a truly simple programming interface for developing powerful, high speed, multi-channel tests, while significantly reducing system development time. A software tool, Test Script Builder, comes with the new SourceMeter instruments, and example programs in the form of built-in TSP test scripts are part of the software. Early studies have shown that by using TSP, and taking advantage of the associated software tools, users can cut development time by a factor of two to four compared to previous generations of test sequencing instruments.

The Models 2601 and 2602 were designed specifically to satisfy electronic manufacturers' needs for cost-effective automated systems that rapidly test high pin count devices or multiple devices in a production test fixture. These SMUs can be used to add new capabilities and capacity to existing test stands easily and lower capital investment in new stands. This is accomplished with easy scalability, simpler system integration, and small test stand footprints. Test systems developed with these new SourceMeter instruments can truly lower the cost of ownership while increasing flexibility, performance, and reliability.

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